REMARKS

This amendment is responsive to the Office Action dated December 28, 2004. Applicants have amended claims 1, 2, 7, 9, 11-15, 18, 24, 30-32, 34 and 35, and cancelled claims 10 and 33. Claims 1-9, 11-32, 34 and 35 are pending upon entry of this Amendment.

As a preliminary comment, it appears the Examiner inadvertently included claims 2 and 3 in the rejection under 35 U.S.C. 102(e). Although initially listed as rejected under 35 U.S.C. 102(e), the Examiner failed to comment on these claims. Instead, the Examiner discussed claims 2 and 3 with respect to 35 U.S.C. 103 (a). For purposes of this response, Applicants assume claims 2 and 3 stand rejected under 35 U.S.C 103(a). Applicants respectfully request clarification from the Examiner on this point.

Claim Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1, 4-9 and 12-17 under 35 U.S.C. 102(e) as being anticipated by Sugai et al. (USPN 6,671,277). Applicants respectfully traverse the rejection to the extent such rejection may be considered applicable to the amended claims. Sugai et al. ("Sugai") fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

Claims 1, 4-8

Applicants' claim 1, as amended, is directed to a routing component that includes a first interface to communicate data with a first network interface and a second interface to communicate data with a second network interface, wherein the first interface and the second interface are integrated within a single integrated circuit. Amended claim 1 further requires the routing component to include an embedded memory within the integrated circuit to buffer data communicated in a first direction from the first interface to the second interface, and a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface to the first interface.

As described in the present application, a router architecture buffers data forwarded in one direction (e.g., inbound data) differently from data forwarded in an opposite direction (e.g., outbound data). For example, pg. 6, ll. 8-16 of the present application states:

> *In the scalable router arrangement, data communicated from a faster interface to a slower interface is stored in an external memory associated with the routing component that received the data. Thus, for example, data received via the crossbar arrangement is buffered in the external memory before being output via a WAN interface. Data communicated from the WAN interface to the crossbar arrangement, on the other hand, is stored in an embedded memory device. ...*

Thus, as illustrated by this example, the described routing architecture may utilize an internal embedded memory when forwarding data from a slower interface (e.g., a WAN interface) to a faster interface (e.g., a switch fabric). However, the same routing component may use an external memory when forwarding data in an opposite direction from the faster interface to the slower interface.

In general, Sugai describes a router having a plurality of routing processors 10 coupled by a crossbar switch 20. According to Sugai, each of routing processors 10 includes a transfer engine 13, a search engine 14, a header RAM 11, a packet buffer 12, a route table 15, an ARP (address resolution protocol) table 16, and a filter/QoS (flow search table) 17.[1] Sugai states that "[t]he search engine 14 is configured with "an exclusive LSI (Large Scale Integrated Circuit) or the like hardware capable of high-speed processing."[2] Thus, contrary to the Examiner's assertion, this statement at least implies that header RAM 11 and packet buffer 12 are separate integrated circuits and, therefore, are not embedded memories.

Moreover, Sugai makes clear that header RAM and packet buffer 12 are used to buffer packet data in the same manner when transferring inbound packets and outbound packets. For example, with respect to FIG. 3, Sugai states:

> *First, when a packet is input to a first network interface 30 through the network through a port, the first network interface 30 transmits it to the transfer engine 13. The transfer engine 13 stores the received packet in the packet buffer 12 (S301). Also, the transfer engine 13 extracts only the header of the input packet and by adding the internal header, forms header information, which is stored in the header RAM 11 (S301). ...*
>
> *In the transfer engine 13, an output packet is produced (S305) based on the packet stored in the packet buffer 12 and the header information (including the transfer control*

[1] Col. 5, ll. 8-13.
[2] Col. 5, ll. 14-17.

> *information) stored in the header RAM 11. The transfer engine 13 outputs the output packet thus produced to the destination. **In the case where the transfer route is associated with any other routing processor 10, the transfer engine 13 sets the packet in queue for the buffer of the particular other routing processor 10, while in the case where the transfer route is associated with the network interface 30 of the local routing processor 10, the transfer engine 13 sets the packet in queue for the corresponding port 40** (emphasis added).*

Thus, Sugai fails to teach or suggest a routing component having an embedded memory within an integrated circuit to buffer data communicated in a first direction from the first interface to the second interface, and a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface to the first interface, as required by amended claim 1. Quite the contrary, Sugai utilizes the same buffering scheme for inbound packets forwarded from the network interface to the crossbar switch and for outbound packets forwarded from the crossbar switch to the network interface. Sugai contains no teaching or suggestion of a routing component that utilizes different buffering schemes when forwarding packets in opposite directions between the same two interfaces.

With regard to claims 4 and 5, Sugai fails to teach or suggest a routing component that utilizes an embedded memory to buffer data received from a wide area network (WAN) and forwarded to a switch fabric, and that utilizes an external memory to buffer data received from the switch fabric and forwarded to the WAN.

With regard to claim 7, Sugai fails to teach or suggest a routing component that is implemented using a single application specific integrated circuit (ASIC). As described above, Sugai states that "[t]he search engine 14 is configured with "an exclusive LSI (Large Scale Integrated Circuit) or the like hardware capable of high-speed processing."[3] This clearly indicates that header RAM 11 and packet buffer 12 are separate from the integrated circuit containing the search engine 14. Consequently, Sugai fails to describe a routing component that is implemented using a single ASIC, as required by claim 7.

Claims 9, 12-17

Independent claim 9 is directed to a network element having a first network interface, a second network interface, and a routing component formed in an integrated circuit, wherein the routing component has an embedded memory within the integrated circuit. Claim 9 further

[3] Col. 5, ll. 14-17.

requires a second memory external to the routing component, wherein the routing component buffers data in the embedded memory that is communicated in a first direction from the first network interface to the second network interface, and wherein the routing component buffers data in the second memory that is communicated in a second direction from the second network interface to the first network interface.

In contrast, Sugai describes a routing processor that utilizes a packet buffer and a header RAM to buffer packets. Sugai makes clear that the routing processor uses the same buffering scheme for inbound packets forwarded from the network interface to the crossbar switch and outbound packets forwarded from the crossbar switch to the network interface. Sugai contains no teaching or suggestion to utilize different buffering schemes when forwarding packets in opposite directions between the same two interfaces.

Consequently, Sugai fails to teach or suggest a routing component that buffers in an embedded memory data that is communicated in a first direction from the first network interface to the second network interface, and buffers in an external memory data that is communicated in a second direction from the second network interface to the first network interface, as required by Applicants' amended claim 9.

Similarly, Sugai fails to teach or suggest a routing component that utilizes an embedded memory to buffer data communicated in a first direction from a WAN to a switch fabric, and utilizes an external memory for buffering data communicated in a second direction from the switch fabric to the WAN, as generally required by claims 12 and 13, respectively.

With regard to claim 15, Sugai fails to teach or suggest a routing component that is implemented using a single ASIC. As described above, Sugai indicates that header RAM 11 and packet buffer 12 are separate from the integrated circuit that contains search engine 14. Consequently, Sugai fails to describe a routing component that is implemented using a single ASIC, as required by claim 15.

Claims 14, 16, 17 depend from claim 9 and are allowable for at least the reasons the reasons states above.

Sugai fails to disclose each and every limitation set forth in claims 1, 4-9 and 12-17. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of

Applicants' claims 1, 4-9 and 12-17 under 35 U.S.C. 102(e) as amended. Withdrawal of this rejection is requested.

Claim Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 2, 3, 10, 11, and 18-35 under 35 U.S.C. 103(a) as being unpatentable over Sugai in view of Erimil et al. (USPN 6,745,246). Applicants respectfully traverse the rejection to the extent such rejections may be considered applicable to the claims as amended. The applied references fail to disclose or suggest the inventions defined by Applicants' claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

Claims 2, 3, 10, 11, 18-29

With respect to independent claims 18 and 24, Sugai fails to teach or suggest an integrated circuit that comprises an embedded memory to buffer data communicated in a first direction from the first interface to the second interface, and an interface to a memory external to the IC for buffering data communicated in a second direction from the second interface to the first interface.

In contrast, Sugai describes a routing processor that utilizes a packet buffer and a header RAM to buffer packets. Sugai makes clear that the routing processor uses the same buffering scheme for inbound packets forwarded from the network interface to the crossbar switch and outbound packets forwarded from the crossbar switch to the network interface

Erimil fails to address these deficiencies of Sugai. In general, Erimil describes a network switch for modifying a bandwidth request between a requestor and a router. As described in reference to FIG. 2, the Erimil switch includes an "integrated multiple port network switch 40" and an external buffer memory 42 for storing frame data. At col. 6, ll. 23-24, Erimil states that buffer memory 42 is used to store data frames while switching logic 52 is processing forwarding decisions for the received data packets. Erimil makes clear that external buffer memory 42 is used to buffer frame data when forwarding the frames between any of the network switch ports 46.

Thus, neither Sugai nor Erimil contain any teaching or suggestion to utilize different buffering schemes when forwarding packets in different directions between the same two

interfaces. As a result, neither Sugai nor Erimil teach or suggest an integrated circuit that comprises an embedded memory to buffer data communicated in a first direction from the first interface to the second interface, and an interface to a memory external to the IC for buffering data communicated in a second direction from the second interface to the first interface, as required by independent claims 18 and 24.

Applicants have amended claim 2 to require that the routing component include a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface, and a second control unit to buffer in the external memory data that is received from the second interface and forwarded to the first interface. In contrast with these requirements, Sugai describes a router in which each routing processor includes a single transfer engine that utilizes the same buffering scheme for inbound forwarded from the network interface to the crossbar switch and outbound packets forwarded from the crossbar switch to the network interface. Similarly, Erimil describes a switch having a single control unit (switching logic 52) that utilizes the same buffering scheme to buffer frame data when regardless of the direction the frame data is forwarded between network switch ports.

With respect to claims 3, 11, 12, 26 and 27, for at least the reasons stated above, neither Sugai nor Erimil teach or suggest a router that utilizes an embedded memory to buffer data communicated in a first direction from a wide area network (WAN) to a switch fabric, and utilizes an external memory for buffering data communicated in a second direction from the switch fabric to the WAN. Moreover, neither Sugai nor Erimil teach or suggest a router that utilizes an embedded memory to buffer data communicated in a first direction from a first interface to a second interface, and utilizes an external memory for buffering data communicated in a second direction from the switch fabric to the WAN, wherein the external memory has a greater storage capacity than the embedded memory.

Claims 30-34

Applicants have amended claim 30 to recite:

A method for communicating data using a network router, the method comprising:
receiving inbound data from a first interface via a first routing component;
buffering the inbound data within an embedded memory internal to the first routing component;
forwarding the inbound data from the first routing component to a second routing component via a switch;

receiving outbound data with the first routing component from the switch;
buffering the outbound data within a memory external to the first routing component; and
forwarding the outbound data to the network first interface.

As discussed above, neither Sugai nor Erimil contain any teaching or suggestion to utilize different buffering schemes when forwarding packets in different directions between the same two interfaces. For at least this reason, neither Sugai nor Erimil teach or suggest the requirements of amended claim 30.

With respect to claim 32, for at least the reasons stated above, neither Sugai nor Erimil teach or suggest: receiving inbound data from wide area network (WAN) via a first routing component; buffering the inbound data within an embedded memory internal to the first routing component; forwarding the inbound data from the first routing component to a second routing component via a switch; receiving outbound data with the first routing component from the switch; buffering the outbound data within a memory external to the first routing component; and forwarding the outbound data to the network first interface.

Claim 35

With respect to claim 35, as described above, neither Sugai nor Erimil teach or suggest a routing arrangement in which at least one routing component comprises: a first interface to communicate data with a network; a second interface to communicate data with the crossbar arrangement; an embedded memory to buffer data communicated in a first direction from the first interface to the crossbar arrangement; and an external memory interface to a memory external to the routing device for buffering data communicated in a second direction from the crossbar arrangement to the network.

For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicants' claims 2, 3, 10, 11, and 18-35 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

CONCLUSION

All claims in this application are in condition for allowance. Applicants respectfully request reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

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